High Performance Nb Josephson Devices for Petaflops Computing

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Abstract—**The Hybrid Technology Multi-Threaded (HTMT) approach to petaflops computing includes large numbers of ultra-high performance Nb Rapid Single Flux Quantum (RSFQ) processor and memory chips, making it by far the largest active superconducting electronics project in the United States. In order to achieve petaflops, RSFQ circuits with 10^5 to 10^6 junctions per chip will be required to operate at clock speeds of 50 to 100 GHz, far beyond the current state of the art. In this paper, we review the state of the art of Nb circuit fabrication and discuss the requirements for significantly improving circuit density and speed.**

Index Terms—**Superconducting Devices, Josephson Junctions, Cryogenic Electronics.**

I. Introduction

THE application of superconducting electronics (SCE) to high performance computing was being actively pursued well before the invention of the integrated circuit. Recognition that Josephson junctions (JJs) offered considerable performance gains over earlier SCE devices came soon after the discovery of the Josephson effect. Experimental investigations of digital Josephson electronics, including the demonstration of sub-ns switching, began in 1966. Fast switching speed and low power dissipation made JJs immediately promising for dense circuits in high-performance digital applications [1],[2].

The low operating temperature requirements of SCE have always pushed interest in digital applications in the direction of large-scale systems. IBM pursued digital SCE for general purpose computing until 1983, after which a major program with similar overall goals began in Japan. Nevertheless, digital SCE today remains in the research stage, while the commercial success of silicon integrated circuits has driven four decades of exponential improvement in speed, circuit density and computing power. However, as semiconductor circuit densities continue their growth, limitations imposed by increasing on-chip power dissipation are expected to lead to a dramatic slowing of the steady increase in processor speeds within the next decade. Thus, digital SCE continues to be pursued as a "technology of the future" for high performance switching and computing applications [3].

"Major advances in key technologies present the opportunity to achieve petaflops scale computing within a decade--far less time than anticipated through the evolution of conventional semiconductor technology" [4]. This opportunity led to plans for a petaflops-scale machine incorporating superconductor, semiconductor and optical logic, memory and communications technologies based on the Hybrid Technology Multithreaded (HTMT) architecture. The core of the proposed HTMT machine are Rapid Single Flux Quantum (RSFQ) JJ processors. Although "the large disparity in access latencies between the fastest superconductor logic and the slowest optical memory present a formidable challenge to efficient system use...the hybrid technology architecture features new multihtreading techniques to manage the much greater latencies that result from the combination of the new technologies" [4].

The HTMT approach to petaflops computing is not merely a final attempt at a JJ-based computer with existing technology. It will require developments that go well beyond the current state of the art. This paper addresses the prospects for advanced JJ devices that could enable significant improvement of SCE circuit speeds.

II. Historical Overview

A. Digital SCE Technology

Digital SCE technology evolved rapidly from cryotron to JJ-based circuits [1],[2]. Since the late 1970s, both latching and non-latching circuits have been based on SQUID loops. Until 1981, most digital SCE work employed Pb and Pb-alloy JJs [5]. Since that time, Nb has been the dominant material [6],[7]. NbN JJ technology allows operation at ≈10 K, but only for applications requiring no more ≈2000 JJs per chip [8]. High temperature superconducting digital circuits are in a primitive state of development, and fundamental issues appear to limit their operation to relatively low temperatures. The present discussion will concentrate on Nb technology operating at 4 K.

Digital SCE fabrication is based on stable, uniform and reproducible JJs with critical small current variations ($\sigma \approx 1$ to 2% on chip, ≈5% on wafer and ≈10% wafer-to-wafer). A discussion of complete circuit processes is beyond the scope of this paper, and the issues are widely discussed in the literature [6],[7],[9]-[11]. For our purposes it is sufficient to note that practical circuits require integration of JJs with resistors, inductors and several levels of superconducting wiring, with appropriate control of all relevant parameters.

As early as 1983, IBM had a well-characterized Nb-Pb alloy edge junction-based fabrication process [12],[13] deemed adequate for a 4K memory demonstration planned for 1985 [14]. It also demonstrated an all-Nb junction technology [15]. A Nb-Si-Nb "trilayer" JJ process, with

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junctions grown on an entire wafer and then patterned subtractively, was pioneered at Sperry, beginning in the late 1970s [16]. Since the early 1980s, the dominant SCE technology has been based on a Nb-Al_2O_3-Nb trilayer process first demonstrated by Gurvitch *et al.* at AT&T [17]. This process is considered superior to all other processes demonstrated to date, being significantly easier to implement than its predecessors and yielding highly uniform and reproducible devices with nearly-ideal tunneling characteristics. (High junction quality, indicated by low subgap "leakage," is usually been viewed as essential. As discussed below, it is relatively unimportant, perhaps even detrimental, for RSFQ.) Today, the Gurvitch process is the basis for all Nb circuit work [6],[7],[9].

There have been several other significant changes in the state of the art in SCE since the mid-1980s. These include: (1) The complete elimination of Pb alloys in wiring. (2) Reduction of minimum feature sizes to roughly 1 μm. (3) The use of larger chips (from 6 mm to ≥1 cm) and wafers (from ≈50 mm to ≈100 to 150 mm). (4) Planarization of some thin film layers. However, there are two important areas in which the technology has not advanced significantly: (1) The number of film layers in a complete process (4 levels of superconducting wiring) has not changed since before 1980. Several additional wiring levels will be necessary for the advanced circuits required by HTMT. (2) Device areas and current densities remain at or below 1983 levels.

JJ circuit performance increases monotonically with increasing J_c and decreasing junction size. Deep-sub-μm , 20 $mA/\mu m^2$ Nb JJs were demonstrated by 1980 [18]. Experimental μm and sub-μm JJs JJ circuit processes have been developed [7],[19], but they are not used to fabricate complex circuits. Thus, the 1983 IBM circuit process, based on 40 to 80 $\mu A/\mu m^2$, 1.6 to 3.2 μm^2 JJs, remains on a par with today's state of the art. Indeed, a 4K memory, the immediate goal of the IBM program when it ended, is arguably the most impressive digital SCE chip demonstrated to date [7],[20]. In the US, today's most advanced circuit process is based on 40 $\mu A/\mu m^2$, 2.4 μm^2 (minimum area) JJs and was first applied to circuit fabrication in 2000 [9],[10].

There are many reasons why SCE technology has not evolved more rapidly. Following the closing of the IBM program, US and Japanese groups started from scratch. Sophisticated processes took years to develop. For many of the niche applications being explored, impressive performance was possible using 10 to 20 $\mu A/\mu m^2$, 5 to 10 μm^2 JJs, which were also sufficient to develop RSFQ, a new approach to logic, to its present state. Thus, 75% of the SCE results reported at the 1998 Applied Superconductivity Conference (both Nb and NbN) were obtained with chips fabricated at the Hypres, Inc. foundry [21] using a such process [22]. This level of process sophistication was possible in facilities costing a tiny fraction of IBM's investment, but neither technical incentives nor funding were sufficient to drive further process development.

Thus, contrary to widely-held opinion, fabrication technology has not represented a significant limitation to applying SCE to digital computing since the late 1970s. While important process developments have occurred since that time, they did not enable digital SCE, which had already been impressively demonstrated. The most immediate problem contributing to the cancellation of the IBM Josephson program in 1983 was the lack of extendibility of existing 4K memory designs to beyond 16K [14], a problem that persists to this day for latching circuits. In general, the latching logic schemes that dominated until recently were constrained to operate at clock speeds much slower than intrinsic JJ switching speeds. Although individual junctions can switch in ps, clock speeds in latching circuits are limited to ns time scales [3],[23]. This severely limited the credibility of large-scale SCE. The emergence of Rapid Single Flux Quantum (RSFQ) in the 1990s [23] has changed that picture, and the possibility of petaflops computing based on RSFQ processors has provided a new motivation for dramatic improvements in the state of the SCE art.

B. The Emergence of RSFQ

It has long been recognized that non-latching JJ circuits are possible, but RSFQ represents the first truly successful effort in that direction [21]. RSFQ circuits are based on the quantized pulses produced by overdamped Josephson junctions. The integrated voltage in an SFQ pulse is the superconducting flux quantum $\Phi_0 = 2.07$ mV-ps. Since the characteristic voltages in a Nb tunnel junction (TJ) can be as large as ≈2 mV, pulses of ps duration are possible, suggesting circuit clock speeds of hundreds of GHz. As with earlier SCE, the advantage over semiconductor technology results from this high switching speed and from extremely low power dissipation. RSFQ has been pursued seriously only since the early 1990s, and its state of development is primitive compared to silicon technology. Yet, it has already become the only demonstrated technology capable of providing dense circuits operating at clock speeds 1 to 2 orders of magnitude faster than semiconductor ones [3]. Even with 3.5 μm design rules, 1 to 2 orders of magnitude larger than those of commercial Si devices, RSFQ digital circuits have been demonstrated at clock speeds of up to tens of GHz. These include high resolution [24] and high speed [25] A/D converters as good as and superior to semiconductor ones, respectively.

Compared with silicon, today's RSFQ technology offers very low device counts. However, shrinking feature sizes will lead to dramatic improvement in circuit density. Device performance also improves as junction sizes are reduced, and simple circuits have been demonstrated at speeds up to 770 GHz. [26]. The HTMT project has already driven [27] the first significant improvement in RSFQ fabrication technology in the past decade [10] but realizing the full potential of the technology in applications such as petaflops-scale computing will require considerable additional improvements, including the incorporation of submicrometer junctions [28]. Fortunately, RSFQ allows superior performance using fabrication technology a generation or more behind Si, allowing commercial Si technology to be leveraged and

saving enormously on development costs.

C. RSFQ in HTMT

RSFQ processors and memory are central to the aforementioned HTMT architecture-based plans for petaflops computing [3],[4]. A description of the HTMT approach is beyond the scope of this paper but is available elsewhere [4],[29]. For our present purposes, it is sufficient to note that a petaflops scale machine would require as many as 10^4 processors, each containing in excess of 10^5 Josephson gates (in this context, a "gate" consists of approximately 10 JJs) and clocked at 50 to 100 GHz. This will require major advances in SCE fabrication and packaging technology. We concentrate here on chip technology, particulary the JJs themselves.

Although an array of 10^6 JJs was reported in 1986 [30], today's state of the art in functional digital circuits is ≈20000 JJ/cm^2 [7]. This is currently being pushed forward by efforts to build 20 to 25 GHz RSFQ processor with >50000 JJ/cm^2 [27]. HTMT plans [3],[4],[29] call for adding up to 4 Nb layers to today's 4-Nb level processes [7],[9],[10]. Adding Nb levels with reduced linewidth would significantly increase gate density, requiring the incorporation of planarization [31] into the process.

Here we discuss the prospects for improving JJ performance by reducing device dimensions from 1.75 μm [10] to 0.4 to 0.8 μm [4],[29] and eliminating resistive shunts [28], leading to significantly increased density and clock speed. Believing that an entirely new technology, one not based on Nb-Al_2O_3-Nb JJs, is unlikely in the foreseeable future, we concentrate on improving that process.

III. RSJ MODEL

A. Introduction

The development of RSFQ [3],[23] has been based on the familiar Resistively-Shunted Junction (RSJ) model for Josephson junctions [32]. Within the RSJ model, a junction is taken as a parallel combination of three lumped elements: (1) An ideal supercurrent source obeying $I = I_c \sin\varphi$, I_c is the junction critical current and φ is the quantum-mechanical phase difference across the junction. (2) A resistor obeying Ohm's law $I = V/R$, where V is the voltage drop across the junction and R is the device resistance. (3) A capacitor obeying $I = CdVdt$, where C is the device capacitance. Using the relation $d\varphi/dt = 2\pi V/\Phi_0$, and summing these three contributions to obtain the total device current yields the nonlinear differential equation that describes the junction dynamics and current-voltage characteristic (IVC).

An ohmic resistor poorly describes dissipation in many JJs. The RSJ model can be adapted to incorporate the nonlinear IVCs of superconducting TJs, but this approach has limited utility because it neglects the frequency dependence of the supercurrent [32]. The RSJ model gives a good accounting of JJ behavior provided that $IcR << 2\Delta/e$, where 2Δ is the superconducting energy gap. This has enabled the development of RSFQ technology based on RSJ. However, as circuit speeds increase more refined models based on full microscopic junction theories will be required [34]-[36].

B. Time Scale and Junction Damping

The RSJ model basically describes an L-R-C circuit in which the supercurrent-carrying element is a parametric inductor. Time (and frequency) in the RSJ model is measured in units of L/R:

$$\tau_0 \equiv \frac{1}{\omega_J} = \frac{\Phi_0}{2\pi I_c R}. \tag{1}$$

Traditionally, JJ damping is characterized by McCumber parameter β_c rather than by the usual quality factor Q:

$$\beta_c \equiv Q^2 = \left(\frac{\omega_J}{\omega_P}\right)^2, \tag{2}$$

where the frequency $(LC)^{-1/2}$,

$$\omega_P = \sqrt{\frac{\Phi_0 I_c}{2\pi C}} = \sqrt{\frac{\Phi_0 J_c}{2\pi C'}}, \tag{3}$$

is the Josephson plasma frequency. Here C' = C/A is the specific capacitance of a device of area A

Underdamped JJs ($\beta_c > 1$) have hysteretic IVCs under current bias. RSFQ circuits employ overdamped JJs ($\beta_c < 1$) with single-valued IVCs, although operation in the $\beta_c = 1$ to 2 range is possible, even advantageous (the behavior of JJs in circuits differs in detail from that of individual junctions) [10]. Within the constraint of small β_c, higher I_cR corresponds to faster RSFQ circuit operation, as implied by (1). Thus, as we shall see below, the challenges in advancing JJ technology center on increasing I_cR.

C. Tunnel Junctions Parameters

In an ideal Josephson TJ, I_cR is independent of the tunnel barrier thickness:

$$I_c R_n = \frac{\pi\Delta(T)}{2e}\tanh\frac{\Delta(T)}{2kT} \cong \frac{\pi\Delta(0)}{2e}, \tag{4}$$

where R_n is the device's zero-bias *normal state* resistance [33]. For Nb 4.2 K, $2\Delta \approx 3$ meV so $I_cR_n \approx 2.3$ mV. Typical *measured* I_cR_n values for Nb-Al_2O_3-Nb junctions range from 1.6 to 1.9 mV, although values in excess of 2 mV have been reported in high J_c devices [28],[34].

Because TJ electrodes are separated by ≈1 nm, C' is large. The capacitance of Nb-Al_2O_3-Nb junctions was measured as a function of J_c by Maezawa *et al.* [37]. Their data are summarized by the fit:

$$C' = \left(41.2fF/\mu m\right)^2 \Big/ \left\{1 - 0.18\log_{10}\left[J_c/(1\,\mu A/\mu m^2)\right]\right\}. \tag{5}$$

These values are consistent with those measured by other groups, even when extrapolated to high J_c [28]. For a typical device, with $J_c = 10$ μA/μm^2, C' = 50 fF/μm^2 and $I_cR_n = 2$ mV, we obtain $\beta_c \approx 60$, so the device is underdamped.

D. Hysteresis and External Shunts

Fig. 1 shows, as a function of β_c, the degree of hysteresis, the ratio $\alpha = I_r/I_c$ in a JJ IVC. Here I_r is the current at which the junction returns to the zero voltage state as bias current is reduced from a value exceeding I_c. Curve (a) shows the result obtained from the RSJ model [32],[38]. The IVC of a real superconducting TJ is appreciably more hysteretic than this. For example, $\beta_c \approx 60$ predicts $\alpha \approx 0.2$ while, experimentally, $\alpha \approx 0$. The disparity results from the fact that, in addition to having large β_c values (calculated using R_n as the resistance), the low-bias resistance is actually much larger, typically $\approx 50R_n$ (insofar as "resistance" can be used to describe a highly nonlinear IVC). Curve (b) shows $\alpha(\beta_c)$ at T = 0 obtained from microscopic TJ theory [38] (again with R_n used as the resistance in defining β_c). Note that α rapidly approaches 0 for $\beta_c > 10$. The finite subgap current in a real TJ results in reduced hysteresis, but this effect is not appreciable for Nb devices at 4.2 K.

So, there is a large disparity between isolated, underdamped TJs and the RSJ devices assumed in RSFQ design. Yet RSFQ has been based almost entirely on TJs rather than other weak links, most of which are naturally overdamped. The reason is that earlier JJ logic schemes relied on the highly nonlinear IVCs of TJs. Thus, all practical integrated circuit processes demonstrated to date rely on TJs. In addition, no other weak link has proven to be nearly as uniform, stable and reproducible as the TJ.

TJs suitable for application to RSFQ are obtained by employing external resistive shunts. The same technique has been used for many years to fabricate SQUIDs [39]. Using the above example of a TJ with $J_c = 10\ \mu A/\mu m^2$ and noting that $\beta_c \propto R^2$, we see that β_c is reduced from 60 to 1 by employing a shunt with resistance $0.13R_n$. Since the subgap resistance of the TJ is $>> R_n$, device resistance is ohmic and very close to the shunt resistance for $V < 2\Delta/e$, as the ohmic shunt conductance dominates the TJ subgap conductance even as R begins to approach R_n. Therefore the RSJ model is usually a good approximation and curve (a) in Fig. 1 applies. External shunting is practical as long as the shunt inductance is negligible (although we will neglect it, shunt inductance should be included in any detailed junction model). It has been employed in almost all RSFQ fabrication to date.

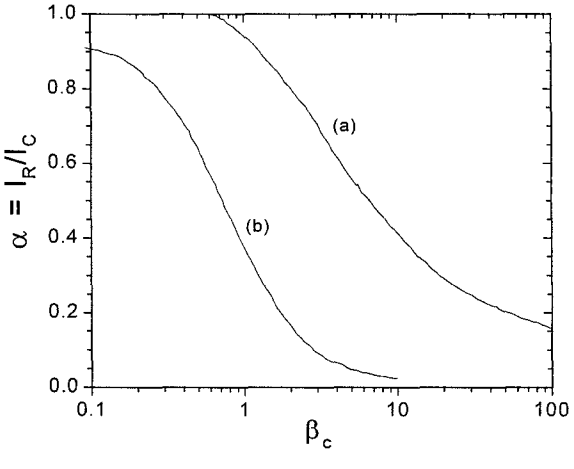

Fig. 1. Hysteresis $\alpha = I_r/I_c$ as a function of β_c in a JJ IVC, as obtained from (a) the RSJ model and (b) microscopic theory.

E. Device and Circuit Speed

The ultimate limit on clock speed in an RSFQ circuit is the width of a SFQ voltage pulse, $\approx 4\tau_0$. In terms of basic device parameters, ω_J and τ_0 can be expressed as:

$$\omega_J = \frac{1}{\tau_0} = \sqrt{\beta_c}\omega_P = \sqrt{\frac{2\pi}{\Phi_0}\beta_c \frac{J_c}{C'}}. \quad (6)$$

This result is general within the RSJ model, applying to any device structure. For fixed β_c, circuit speed depends only on ω_P, or J_c/C'.

The external shunt is chosen to make $\beta_c \approx 1$, or perhaps slightly larger. (Smaller values of β_c would result in reduced speed.) But shunting to achieve overdamping already *reduces* circuit speed from theoretical limits, a compromise deemed acceptable in most work to date because the resulting device performance has been adequate. Interest in applications such as petaflops computing mandates a dramatic increase in clock speeds. Decreasing the thickness of the barrier of a TJ results in a linear increase in C' and an exponential increase in J_c. Therefore, J_c/C' increases almost in proportion to J_c and speed increases almost in proportion to $J_c^{1/2}$. Thus, "high J_c" is equated with high performance.

The simplest RSFQ circuit is the toggle flip-flop. Used as a process benchmark, it can operate at speeds up to $f_J = \omega_J/2\pi$. Using the traditional design criterion $\beta_c = 1$ and (5), a flip-flop fabricated with a state of the art 40 $\mu A/\mu m^2$ circuit process today should run at 230 GHz, consistent with experiment [10]. Increasing J_c to 500 $\mu A/\mu m$ allows operation at 700 GHz, nearly the gap frequency of Nb, consistent with experiment [26].

Functional digital circuits involve timing issues not present in a simple flip-flop. Internal circuit delays, process spreads, noise and other considerations require that SFQ pulses be separated by several times the width of an individual pulse [23]. Thus, the range of speeds reported for RSFQ circuits reported for circuits at a given J_c is large. Empirically, for a variety of asynchronous circuits such as transmission lines, splitters and mergers, the maximum speed is [23]

$$f^{\max} = \frac{1}{15\tau_0} to \frac{1}{10\tau_0}. \quad (7)$$

Delays in more complex clocked circuits are larger, limiting operation to [23],[Lik P.C.]

$$f_{clock}^{\max} = \frac{1}{60\tau_0} to \frac{1}{25\tau_0}. \quad (8)$$

The slower result in (8) was obtained for a 64-bit adder, the most complex circuit thoroughly-simulated to date, using realistic process spreads and including thermal noise [40]. Thus, the slower figure is an indicator of the speed of, say, an entire processor. Note that these results are design-dependent and do not represent physical limits.

IV. High Performance RSFQ Tunnel Junctions

A. Nb-Al_2O_3-Nb Circuit Performance

As with other digital JJ circuits, RSFQ gates involve loops containing one or more JJs with $LI_c \approx \Phi_0$, where L is the loop inductance. Thermal fluctuations contribute to bit error rate (BER), so $\Phi_0 I_c >> kT$. For 4 K circuits with very low BER, the $I_c > 100$ to 125 μA. For $J_c = 10$ μA/μm^2, $I_c = 125$ μA for a 3.5 μm-square JJ (100 μA for a 3.5 μm-diameter circular JJ).

Of course, J_c and A are inversely proportional. Smaller junctions enable higher gate speeds, denser circuits and improved system performance. HTMT should motivate process modernization. In addition to reducing JJ size, an HTMT-level process requires reductions in wire size and pitch and additional wiring levels. These require improved lithography and planarization, which are readily available; the major limitation to significant process upgrades is cost.

Fig. 2 shows the operating frequency ranges given by (7) and (8), along with the maximum speed of a flip-flop, f_J. Table I lists device parameters for several generations of JJ fabrication, assuming a rough doubling of J_c in each. The current state of the art should enables clocked circuits in the 25 to 60 GHz range. With 0.8 μm, 200 μA/μm^2 JJs, 50-120 GHz should be possible. If β_c can be increased to 2 in the relevant circuits with acceptable margins, these speeds would increase by 40%. Combining 0.8 μm JJs with several additional Nb wiring layers may be sufficient for a first-generation petaflops machine.

With $J_c \geq 1$ mA/μm^2, speeds of 100 to 230 GHz should be possible for clocked circuits, with some asynchronous circuits operable up to 400-600 GHz. In principle, shunt resistance should, making bare TJs overdamped, or "self-shunted." Eliminating external shunts would allow dramatic *additional* improvements in circuit density. For still higher J_c, I_cR is independent of barrier thickness. In reality, the nonlinear IVC of a TJ complicates the situation, increasing the J_c required for self-shunting (see below).

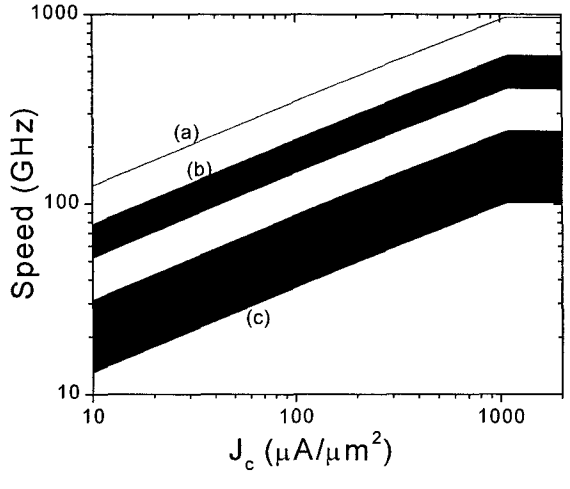

Figure 2: Nb RSFQ circuit speed versus critical current density for Nb-Al_2O_3-Nb technology. (a) The maximum speed of a flip-flop, f_J. (b), (c) The shaded areas indicate the range of speeds given by (7) and (8) for asynchronous circuits and clocked circuits, respectively.

B. Self-shunted Junctions

The idea of self-shunting is an old one. Already in 1980, Nb-Nb_2O_5-Pb_3Bi junctions failed to show self-shunted (i.e., non-hysteretic) behavior even at $J_c > 10$ mA/μm^2 [18]. More recently, substitution of AlN for Al_2O_3 in Nb junctions resulted in hysteretic junctions with low subgap currents, even at 1 mA/μm^2 [41],[42]. In fact, referring to Fig. 1, an ideal TJ should not be self-shunted at any J_c. Thus, although low "leakage" was required for latching logic, high subgap current is *vital* for high J_c RSFQ devices. Thus, there are actually *two* requirements for self-shunting: (1) $\beta_c \leq 1$ and (2) An approximately ohmic IVC.

Fortuitously, the degree of hysteresis in Nb-Al_2O_3-Nb JJs, which is in good agreement with the microscopic theory curve in Fig. 1 for low J_c, crosses over and approaches the RSJ prediction for J_c in excess of roughly 200 μA/μm^2. The high subgap current that allows self-shunting results from multiple Andreev reflections (MAR) [34] which, as J_c increases, come to dominate over simple tunneling as the major conduction mechanism. For high J_c, the IVC, although nonlinear, approximates an Ohmic resistor sufficiently well that self-shunting can occur. Indeed, although not seen for $J_c = 1$ mA/μm^2 as predicted by the RSJ model, self-shunting has been demonstrated at 2 mA/μm^2 [28]. This promising result, and shift register operation at 770 GHz [26], have made deep-sub-μm, high J_c Nb-Al_2O_3-Nb TJs the favored technology for high performance RSFQ digital processors.

C. Junction Physics Issues

MAR requires multiple traversals of the barrier, which is possible only if the quantum transmission probability $|T|^2 \approx 1$. This implies a resistance equivalent to that of a pure metallic contacts. Therefore, only a tiny fraction of the area of a high J_c TJ contributes to MAR. The barrier consists of a conventional tunnel barrier with numerous nm-sized metallic point contacts that come to dominate current transport as J_c increases [34].

Assuming these to be quantum point contacts (QPC), we anticipate that each one will contribute a conductance e^2/h and a critical current of $\approx \pi e\Delta(0)/h$, or 180 nA [43]. If, for a 1

TABLE I
J_c AND JUNCTION PARAMETERS ($\beta_c = 1$)

J_c (μA/μm^2)	Size (μm)	C (fF/μm^2)	f_J (GHz)	I_cR (mV)	asynch f (GHz)	clocked f (GHz)
10	3.54	50	124	0.26	52 - 78	13 - 31
20	2.50	54	169	0.35	71 - 106	18 - 42
40	1.77	58	230	0.48	97 - 145	24 - 58
100	1.12	64	346	0.72	145 - 217	36 - 87
200	0.79	70	468	0.97	196 - 294	49 - 118
500	0.50	80	693	1.43	290 - 435	73 - 174
1000	0.35	90	927	1.92	388 - 582	97 - 233

$mA/\mu m^{2\,JJ}$, QPCs contribute half of the total critical current of 125 μA [34],[28] only 340 QPCs are required. One expects statistical fluctuations in the number of QPCs on the order of $1/n^{1/2} \approx 5\%$, potentially leading to an unacceptable spread in I_c. This matter requires further investigation.

At present, the effect of MAR on circuit performance is only beginning to be understood [35],[36]. Device models incorporating MAR also need to be devised and verified. The breakdown of other aspects of the RSJ model due, for example, to the presence of voltages approaching the superconducting gap, also require consideration.

D. Alternatives to the High J_c TJ: Weak Links

Simple digital circuits based on high J_c TJs have been demonstrated. The development of a complete circuit process, although it will require considerable effort and investment in new fabrication tools, is straightforward in principle. However, questions remain concerning physical limits on JJ parameter spreads and the details of the behavior of MAR-dominated devices in real circuits. For these reasons, alternatives to the high J_c TJ merit consideration.

The Josephson effect is most familiar in TJs, in which the required weak coupling is natural, but other "weak link" structures also show Josephson effects [44]. Most weak links are naturally self-shunted, although I_cR varies with J_c. None has been successfully adapted to digital circuit technology.

For example, replacing a nm-thick tunnel barrier with a normal metal hundreds of nm thick results in a very low-capacitance junction. However, I_cR is generally very small, implying very slow RSFQ devices. Theoretically, high I_cR requires such high J_c that useful digital devices would be prohibitively small. This approach appears unpromising for digital technology, although it has been applied to tunable voltage standards [45] and was seriously considered as a means for obtaining acceptable high T_c JJs [46].

Another alternative approach would replace Al_2O_3 with a smaller barrier height material, reducing capacitance and, according to (6), increasing speed. However, considerable effort was expended in the 1970s on such devices, which were easily supplanted by the Gurvitch process.

As stated earlier, a circuit process based on the complete replacement of Nb-Al_2O_3-Nb JJs is unlikely in the foreseeable future. Two approaches that require relatively minor changes to the fabrication process are therefore of interest.

One approach that may merit further investigation is AlN. Although AlN TJs have capacitance values similar to those of Al_2O_3 ones, AlN appears to allow JJ operation at high J_c values with direct tunneling as the primary transport mechanism. This appears to preclude self-shunted JJs, but any problems that might result from MAR-dominated transport would evidently be avoided with this approach.

Self-shunting occurs only in high-J_c, deep-sub-μm TJs that are outside of the capabilities of mainstream fabrication technology today. One proposed alternative requires only a minor variation in the standard Gurvitch process, the double barrier Nb-Al_2O_3-Al- Al_2O_3-Nb superconductor-insulator-normal-insulator-superconductor (SINIS) JJ. SINIS JJs have received considerable attention recently as potential digital devices [47]. SINIS devices are fabricated by depositing a thin Al layer on top of the Al_2O_3 tunnel barrier and oxidizing it. Empirically, SINIS JJ IVCs are "washed out," and self-shunted junctions have been reported [47]. I_cR products reported to date, however, have been rather low.

Conceptually, a SINIS JJ can be viewed as a SIS TJ with the barrier split in half. (Presumably, each barrier in a SINIS JJ is half as thick as the barrier in an equivalent SIS JJ.) The simplest picture of the device recognizes that, since supercurrent is coherent, $I_c \propto (|T|^2)^2$, where $|T|^2$ is the tunneling probability for a single barrier (the N layer has negligible effect if it is thin). On the other hand, the normal conduction is incoherent and occurs in two steps, so that the conductance $1/R \propto |T|^2$. Therefore $I_cR \propto J_c^{1/2}$. The main effect of splitting the barrier is to lower I_cR. Hysteresis is reduced, both because β_c is low and because leakage is large, but self-shunted SINIS are only possible because they are slow (small ω_J).

From a process viewpoint, control of SINIS I_c requires controlling two oxidation steps rather than the usual one. Since uniformity and reproducibility are issues with all processes, this is a decided disadvantage. In order to achieve a useful J_c of 10 to 1000 $\mu A/\mu m^2$, the two individual barriers must have much higher J_c, well into the MAR-dominated regime. The effect of this mechanism on device behavior has not been analyzed to date.

More fundamentally, we saw in (6) that RSFQ circuit speed depends on the ratio J_c/C'. There simply isn't any other parameter to adjust. The capacitance of a "split barrier" is not significantly different from the capacitance of a single barrier with the same J_c. Therefore, high speed devices require the same high J_c values as SIS TJs. Ultimately, compared with an SIS TJ, an SINIS device is simply a more complex means to the same end, high J_c junctions.

V. Conclusions

Realizing the full potential of RSFQ technology in applications such as petaflops-scale computing will require considerable improvements in superconducting chip fabrication technology. The goal of attaining the ultimate circuit speed translates into a need to obtain the highest possible I_cR product in overdamped Josephson junctions. This can only be accomplished by substantially increasing the ratio J_c/C' (i.e., the plasma frequency) far beyond what is available today. Plans call for increasing J_c in Nb-Al_2O_3-Nb junctions from 40 $\mu A/\mu m^2$ to between 200 $\mu A/\mu m^2$ and >1 $mA/\mu m^2$. This approach has been demonstrated in the laboratory and appears promising, with no fundamental limits preventing implementation. However, considerable work, both on implementing the required process and on understanding the behavior of the junctions, is required.

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